A MODEL-BASED APPROACH TO MASTERING COMPLEXITY IN FPGA-SoC SOFTWARE DEVELOPMENT

MPSI TECHNOLOGIES

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Introduction

Me and MPSI Technologies

- Diploma in Electrical Engineering
- Based in Munich

- R&D Engineer at Mynaric (FPGA-based error-correction algorithms for free-space optical laser communications)

- Founder and Director at MPSI Technologies
- MPSI Technologies: make Embedded Software development more fun by replacing repetitive tasks by model-based source code generation

FPGA-SoC landscape

Devices and applications

Product lines

Selection discussed here: CPU complex can run Embedded Linux

AMD XILINX ZYNQ

- from 2011: Zynq 7000 with Dual 32-bit ARM CPU and SRAM-based FPGA, internally connected via AXI
- from 2016: Zynq UltraScale+ with Quad 64-bit ARM CPU and additional real-time cores / accelerators

intel CYCLONE STRATIX

- from 2012: CycloneV with Dual 32-bit ARM CPU
- from 2016: Stratix 10 with Quad 64-bit ARM CPU

MICROCHIP Microsemi Product Portfolio

RISC-V

- from 2019: PolarFire SoC with Quad 64-bit RISC-V CPU and antifuse-based FPGA

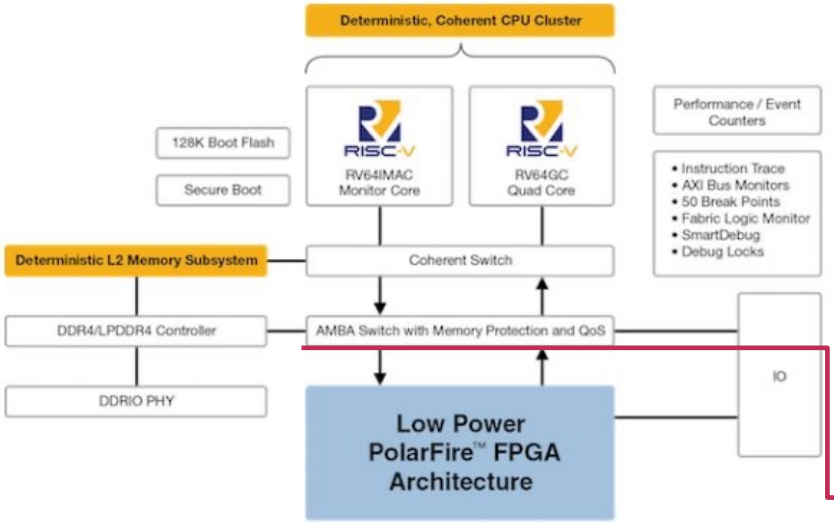
Typical applications

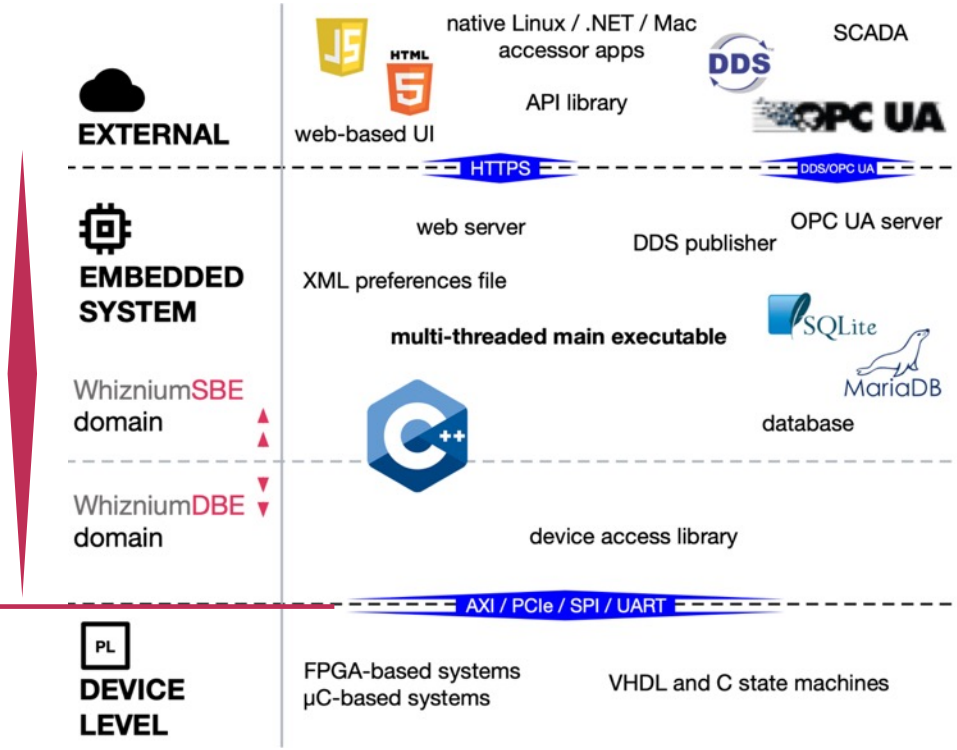
- classical FPGA applications where additional high-level control is of advantage
- ”data reduction” or pre-processing of high-bandwidth sources
- cameras: binning, pixel-level filters, compression, feature and object detection
- ADC’s: spectral analysis, DSP filters
- clock-precise signaling for mixed-signal ASIC’s
- not considered here: data center and hardware acceleration applications

The FPGA-SoC software full stack

From VHDL to C++ to HTTPS and XML

Microchip PolarFire SoC Block Diagram

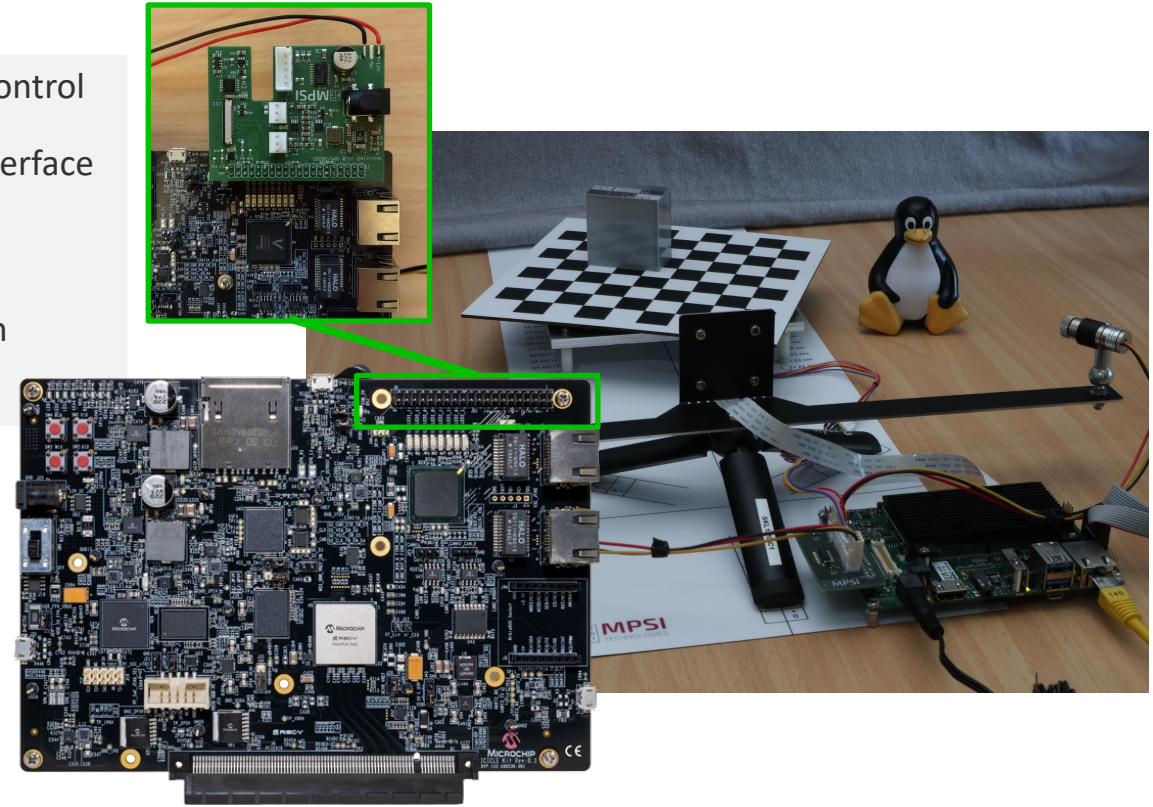




Demo project: hardware

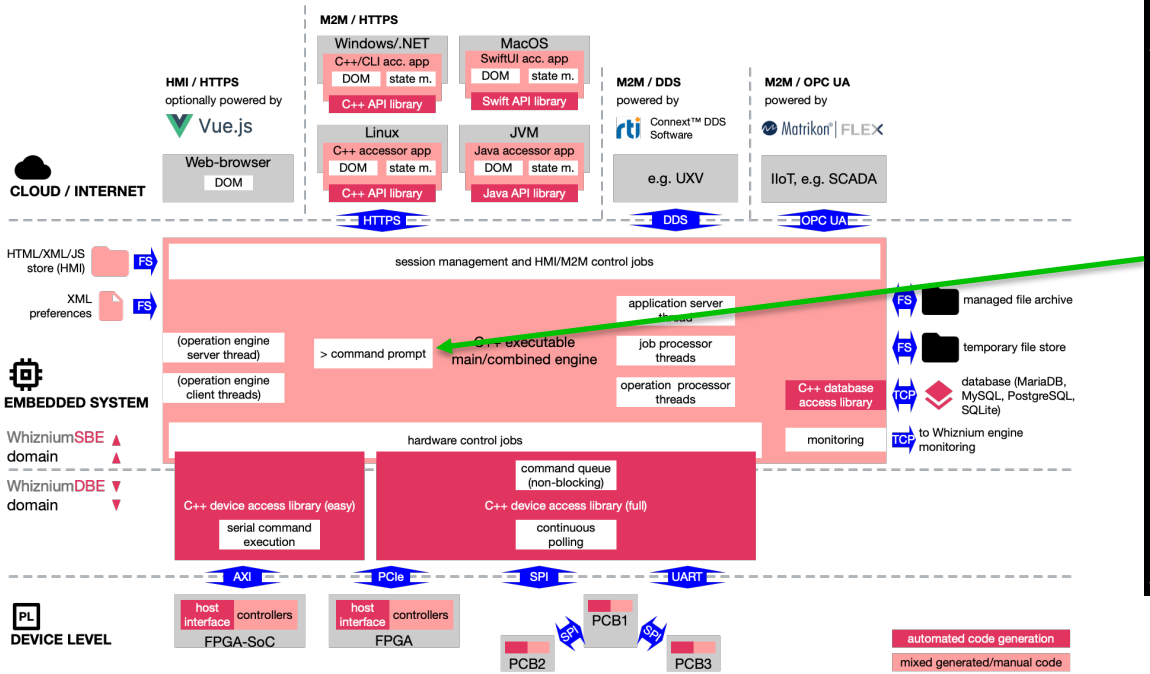
Tabletop 3D laser scanner

- turntable with with stepper motor control
- 5 megapixel camera with MIPI CSI interface
- two intensity-modulated line lasers
- Microchip PolarFire SoC Icicle kit with adapter PCB



Demo project: software

From camera raw data to point cloud display in web browser




```
root@icicle-kit-es:~/whiznium/bin/wzskcmbd# ./Wzskcmbd
Welcome to Whiznium StarterKit v1.0.5!
        starting 4 job processor threads ... {19255, 19256, 19257, 19258} success
        starting 1 operation processor threads ... {19259} success
        starting application server ... success
        starting OPC UA server ... success
Initialization complete.

Wzskcmbd >> showJobs
        + RootWzsk (1)
                - JobWzskSrcV4l2/SRV (2)
                - JobWzskSrcSysinfo/SRV (3)
                - JobWzskSrcFpga/SRV (4)
                + JobWzskIprTrace/SRV (5)
                        - JobWzskActLaser/CLI (6)
                        - JobWzskSrcV412/CLI (7)
                + JobWzskIprCorner/SRV (8)
                        - JobWzskSrcV412/CLI (9)
                + JobWzskIprAngle/SRV (10)
                        - JobWzskIprCorner/CLI (11)
                - JobWzskActServo/SRV (12)
                - JobWzskActLaser/SRV (13)
                + JobWzskActExposure/SRV (14)
                        - JobWzskSrcV412/CLI (15)
                + JobWzskAcqPtcloud/SRV (16)
                        - JobWzskIprTrace/CLI (17)
                        - JobWzskActServo/CLI (18)
                + JobWzskAcqPreview/SRV (19)
                        - JobWzskSrcV412/CLI (20)
                + JobWzskAcqFpgapvw/SRV (21)
                        - JobWzskSrcFpga/CLI (22)
                + JobWzskAcqFpgaflg/SRV (23)
                        - JobWzskSrcFpga/CLI (24)
                + M2msessWzsk (25)
                        - JobWzskSrcSysinfo/CLI (26)
                        - JobWzskIprTrace/CLI (27)
                        - JobWzskIprCorner/CLI (28)
                        - JobWzskActServo/CLI (29)
                        - JobWzskActExposure/CLI (30)
                        - JobWzskActLaser/CLI (31)
                        - JobWzskAcqPtcloud/CLI (32)
                        - JobWzskAcqPreview/CLI (33)

Wzskcmbd >>
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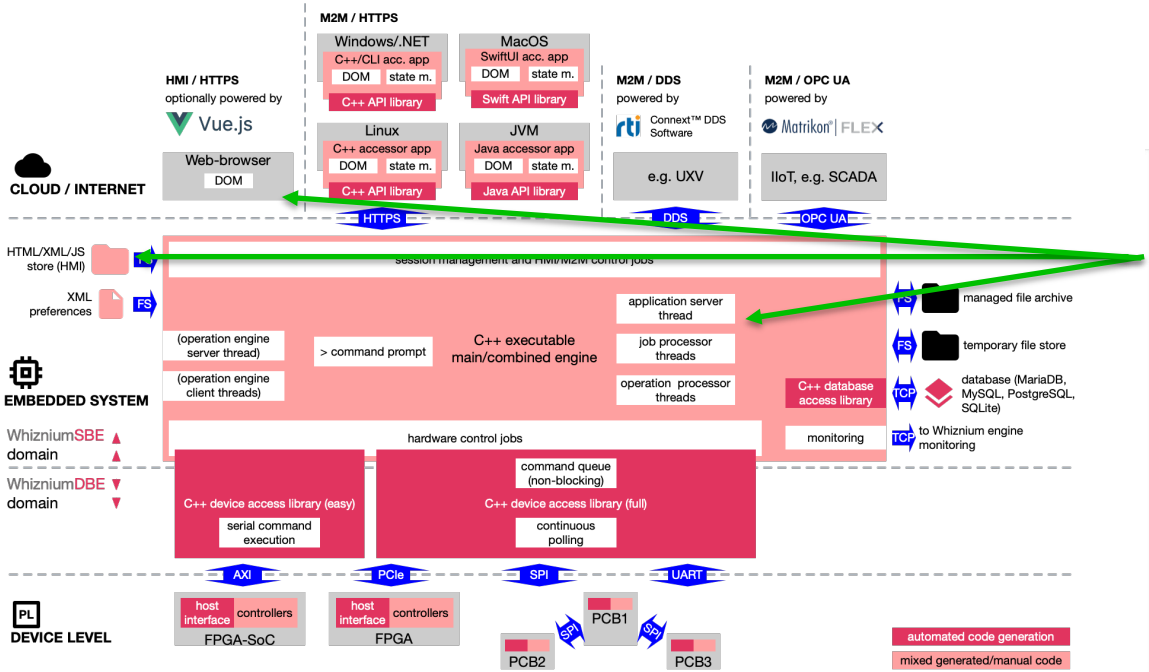

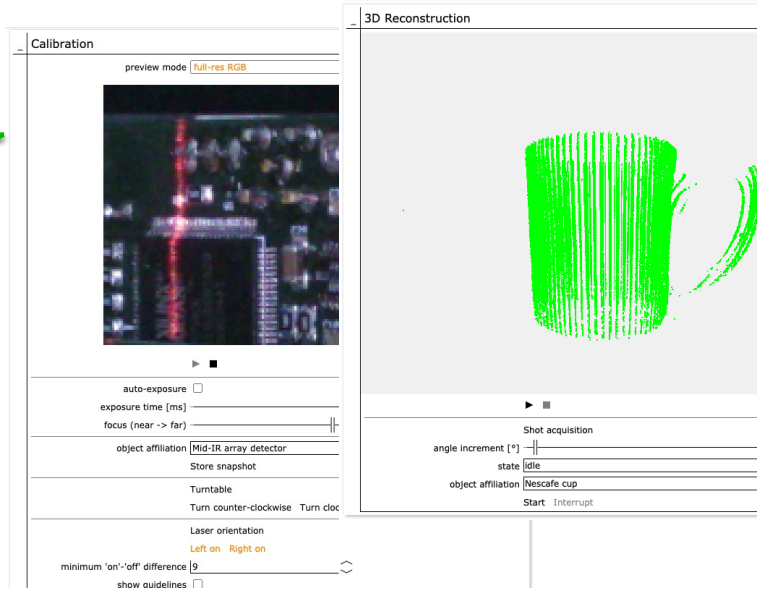

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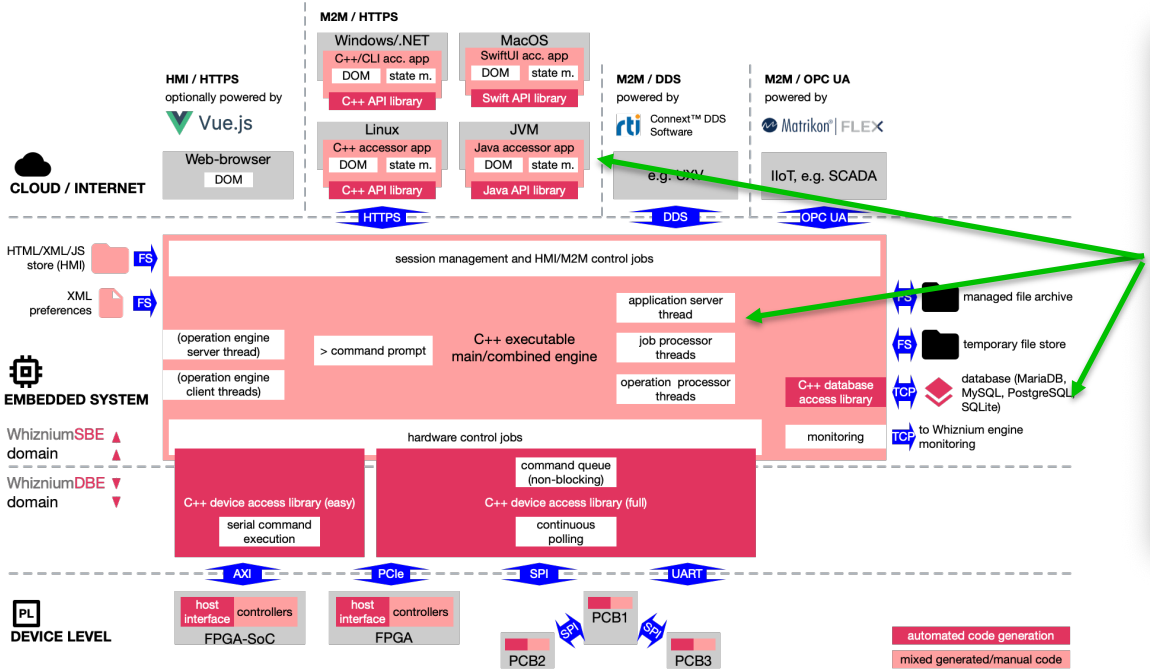

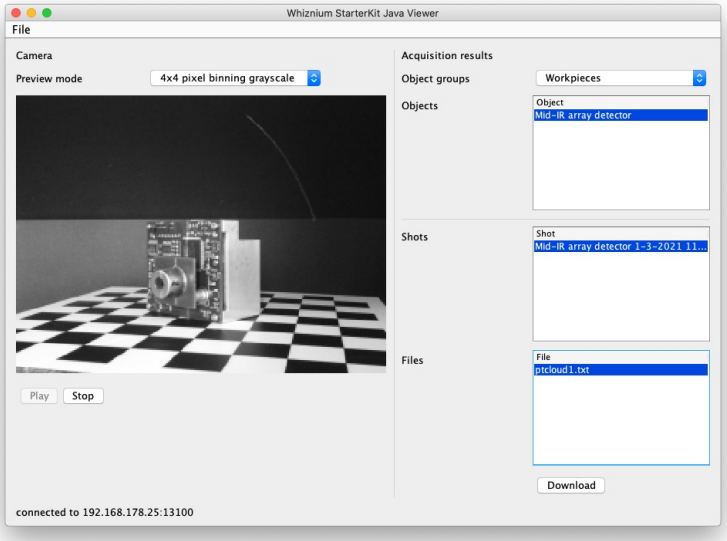

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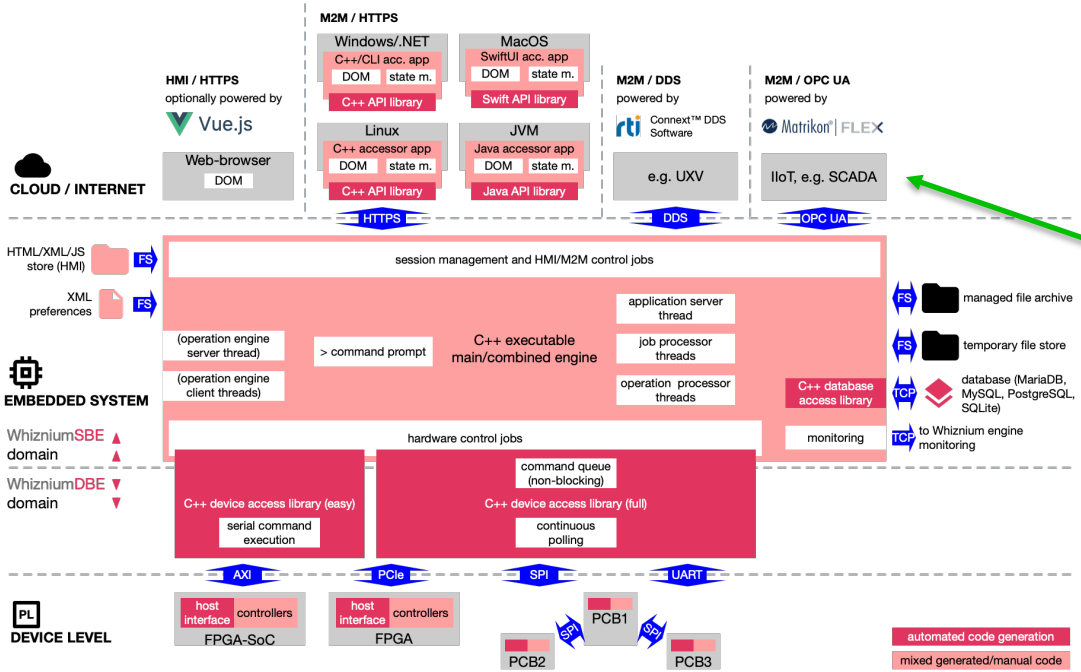

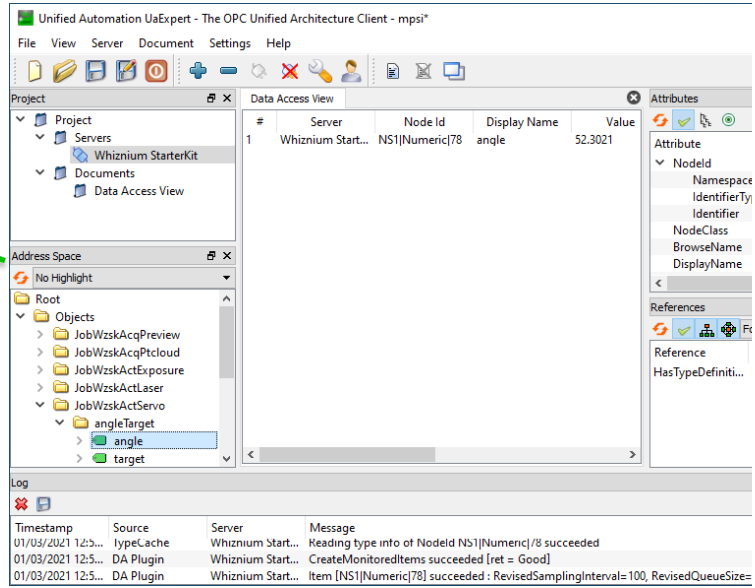

Embedded software model description

WhizniumDBE for FPGA layer, WhizniumSBE for Linux application software

- successive model composition within an SQL database using import (I) and generation (G) steps
- output of source code trees only thereafter
- text-based model files (”diffable”)

WhizniumDBE (Device Builder’s Edition)

- Modular structure (I)
- Command set and buffer transfers (I)
- Data flows and algorithms (I)
- Fine structure (G)
- Custom fine structure (I)
- Finalization (G)

WhizniumSBE (Service Builder’s Edition)

- Deployment information (I)
- Global features (I)
- Database structure (I)
- Basic user interface structure (I)
- Import/export structure (I)
- Operation pack structure (I)
- Custom jobs (I)
- User interface (G)
- Custom user interface features (I)
- Job tree (G)
- Custom job tree features (I)
- Finalization (G)

Deep dive I: from C++ command to RTL finite state machine

Control of turntable stepper motor

- module definition, command definition, fine structure

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Control of turntable stepper motor

IexWdbeMdl v1.1.14								
ImeIMUnit	srefSilRefWdbeMUnit	sref	Title	Easy	srefKToolch	Comment		
fpga	**mpfs250t-fcvg484**	**iccl**	**Microchip PolarFire Soc Icicle kit**	**true**	**libero**			
	ImeIMModule.srefIxVBa	hsrefSupRefWdb	srefTplRefWdbeMModule	sref	Comment			
	wrp		mpfs_ip_AXI_v1_0	**iccl_ip_AXI**				
	top	iccl_ip_AXI	top_mchp_v1_0	**top**				
		ImeIAMModuleP	Val					
		fExtclk	125000					
		extresetNNotP	true					
		ImeIAMModulePar.end						
		ImeIMGeneric.s	Defval					
		fMclk	50000					
		ImeIMGeneric.end						
	...							
	ectr	iccl_ip_AXI;top		**step**	stepper motor control (28BYJ-48 via ULN2003)			
	...							
	ImeIMModule.end							
ImeIMUnit.end								

Deep dive I: from C++ command to RTL finite state machine

Control of turntable stepper motor

IexWdbeCsx v1.1.9											
ImeIMUnit.sref											
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	iccl_ip_AXI;top	**step**									
		ImeIMController.									
		^									
			ImeIMVector2.srefIxVBase	sref	srefsKOption						
			tixlin	VecVWskdIcclStepState	filfed;notit						
				ImeIMVectoritem2.sref	Title	Comment					
				idle							
				move							
				ImeIMVectoritem2.end							
			ImeIMVector2.end								
			ImeIMCommand2.refNum	sref	srefIxVRettype	srefIvrRefWd	srefRvrRef	srefRerR	Comment		
			...								
			0	moveto	void						
				ImeIAMCommandInvpar2.sref	srefIxWdbeVPartype	srefRefWdbe	Length	Defval	srefRefWdbe	Comment	
				angle	uint16			0		in stepper motor steps (4096 per rev.)	
				Tstep	uint8			150		in tkclk clocks: rps = 10000 / (Tstep * 64 * 64)	
				ImeIAMCommandInvpar2.end							
			...								
			ImeIMCommand2.end								
		ImeIMController.end									
	ImeIMModule.end										
ImeIMUnit.end											

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ImeIMUnit.sref												
iccl												
	ImeIMModule.hsrefSup	sref										
	iccl_ip_AXI;top	**step**										
		...										
		ImeIMProcess.sref	clkSrefWdbel	asrSrefWdbeMS	Falling	Syncrst	Extip	Comment				
		op	mclk	reset	false	state(init) or (sta	false	main operation				
			ImeIMFsm.									
			^									
				ImeIMFsmstate	sref	Extip	Comment					
				0	init	false						
					ImeIAMFsm:	Cond1	Ip1	Cond2	Ip2	Cond3	Ip3	Cond4	Ip4
					inv	reqInvMoveto	moveto					
					inv	reqInvSet	set					
					inv	reqInvZero	zero					
					ready	else						
					ImeIAMFsmstateStep.end							
				0	ready	false						
					ImeIAMFsm:	Cond1	Ip1	Cond2	Ip2	Cond3	Ip3	Cond4	Ip4
					runB	Tstep/=0		not targetNotSteady and rng	steady				
					runB	Tstep/=0		targetNotSteady and not atTarget	target				
					ready	Tstep/=0		else	hold				
					ImeIAMFsmstateStep.end							
				...								
				ImeIMFsmstate.end								
			ImeIMFsm.end									
		ImeIMProcess.end										
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- Linux side developer-facing: executable API method

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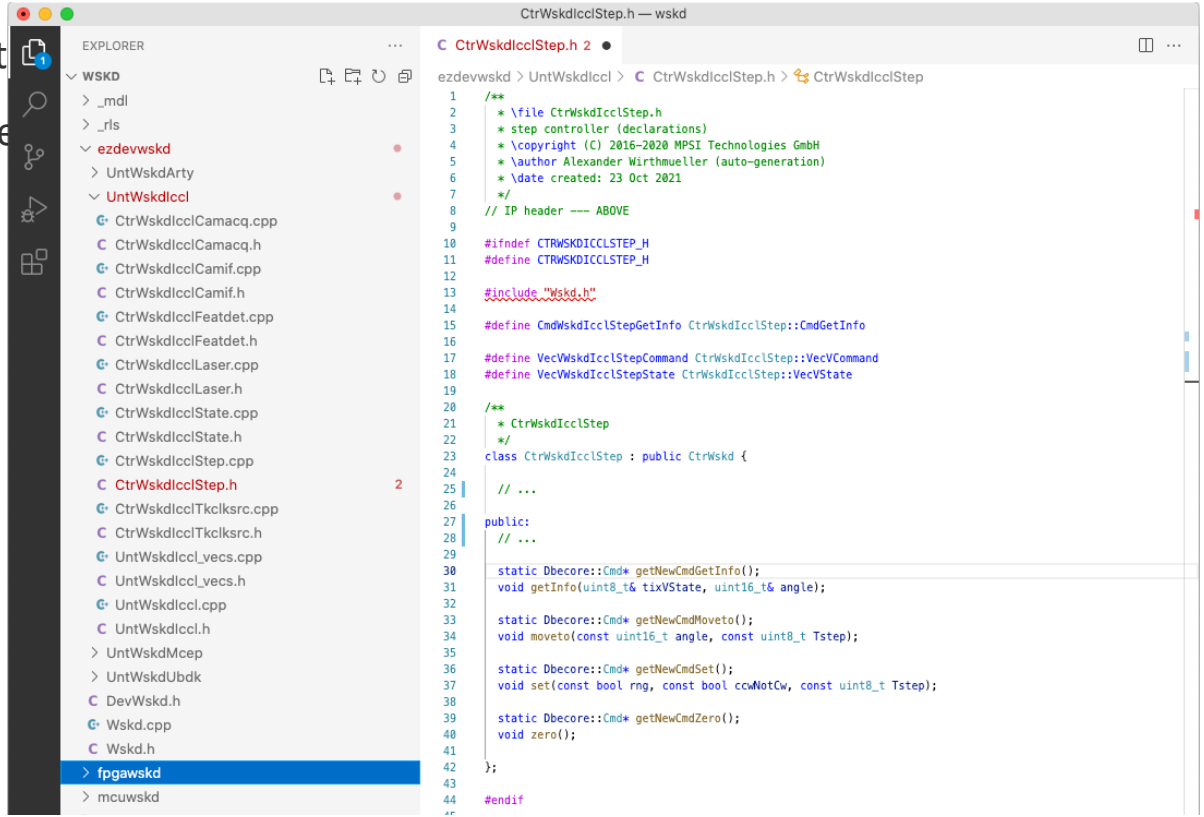

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- Linux side in background: translation into byte code and invocation of character device driver (AXI)
- FPGA side in background: reception and decoding of byte code in “host interface” module, CRC evaluation
- FPGA side developer-facing: handshake signals

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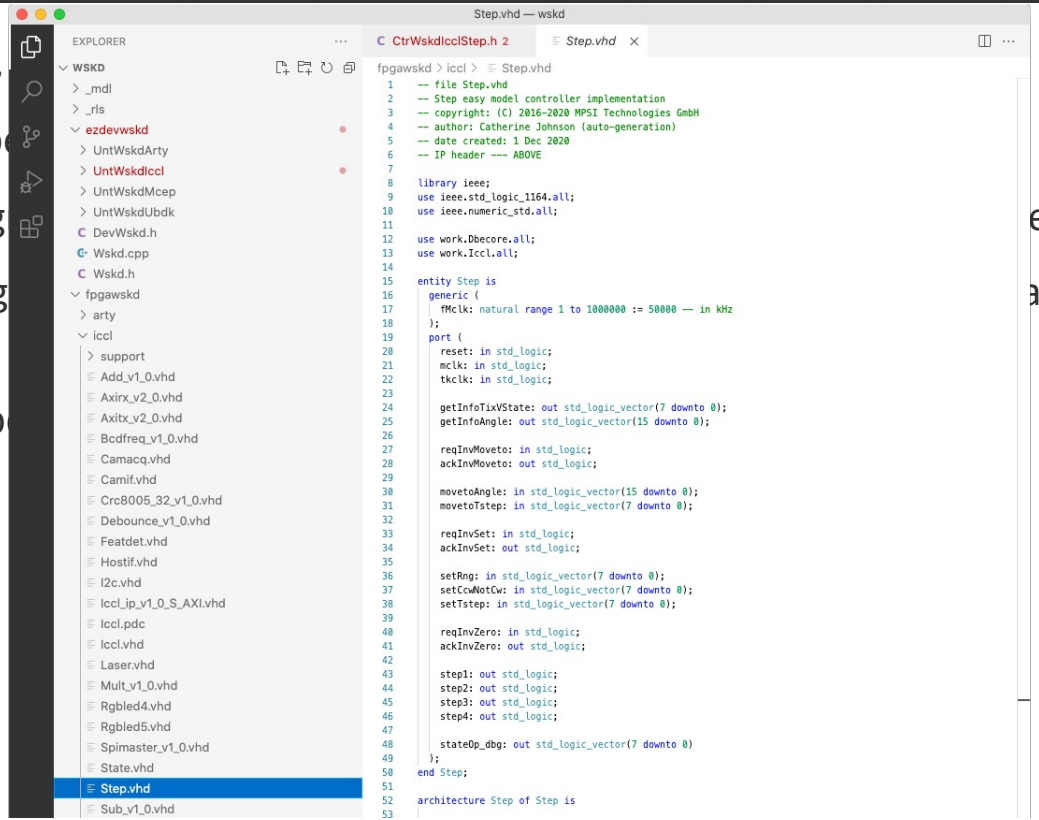

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- FPGA side left for manual implementation: finite state machine reacting to command invocation

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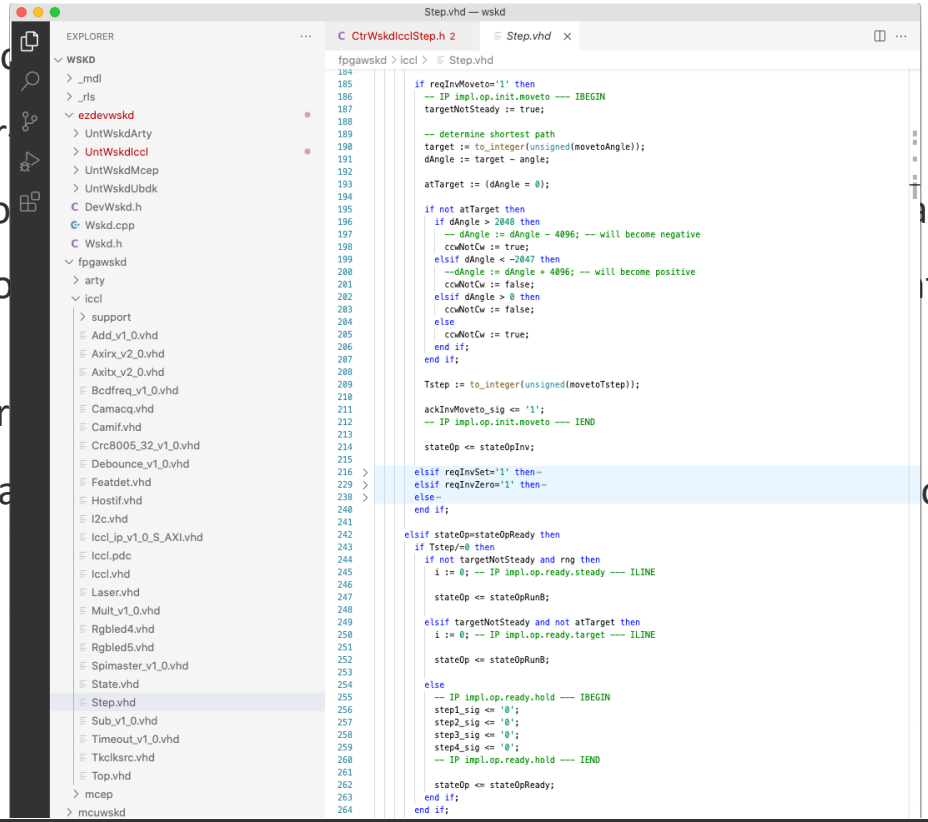

Deep dive II: camera preview images on the move

FPGA-based binning, processing in C++ code and forwarding to the UI

- pixels arrive over four-lane MIPI CSI at 576Mbps per lane and get deserialized into a 10-bit RAW10 data stream at about 20fps
- four preview modes (2560 x 1280 to 160 x 120 RGB vs. 2048 x 1536 to 256 x 192 grayscale), manual implementation using finite state machines and 2/4kB buffers
- ”buffer transfers” are besides “commands” the second functionality which can be generated for the host interface
- polling in separate thread on host, insertion into ”job tree” via “call”
- generation of XML block containing image data, Base64 coded transmission
- reception in web browser via HTTPS/1.1 “long polling”, rendering in HTML5 <canvas/>

Deep dive III: meta data and the “lowering” process in Whiznium

From SQL database structure to code and UI elements to XML/JSON blocks

- all WhizniumSBE applications are backed by a SQLite3 database
- “Database structure”: tables “Object group” (1:N) “Object” (1:N) “Snapshot” and corresponding ”Basic user interface”

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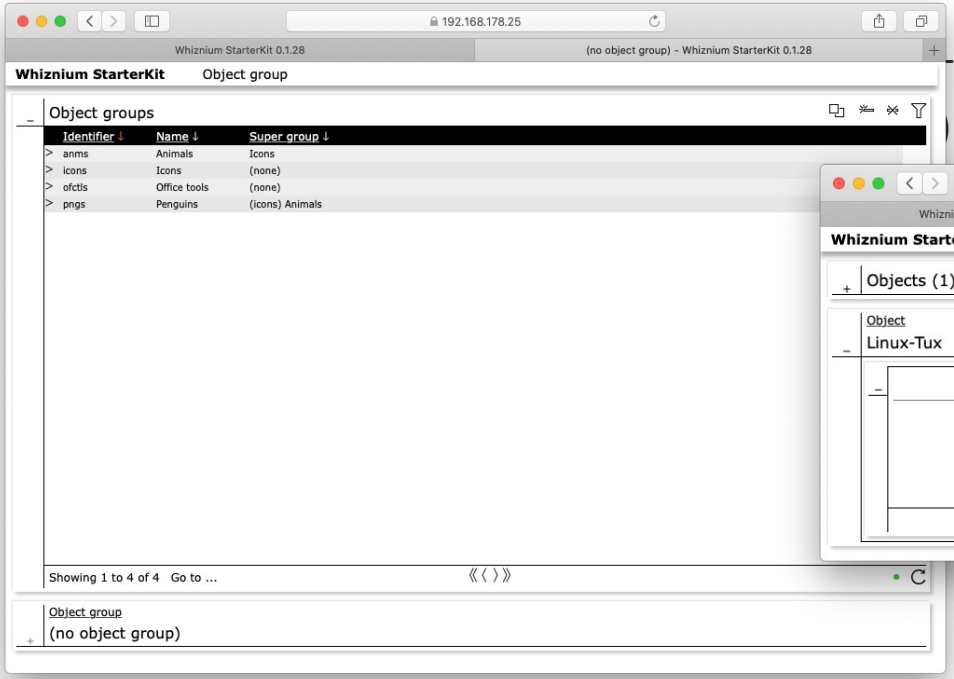
From SQL database structure to code and UI elements to XML/JSON blocks



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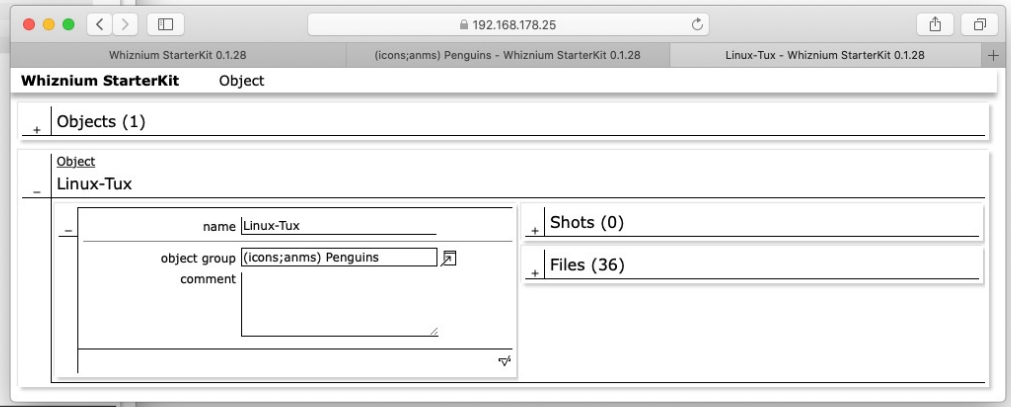

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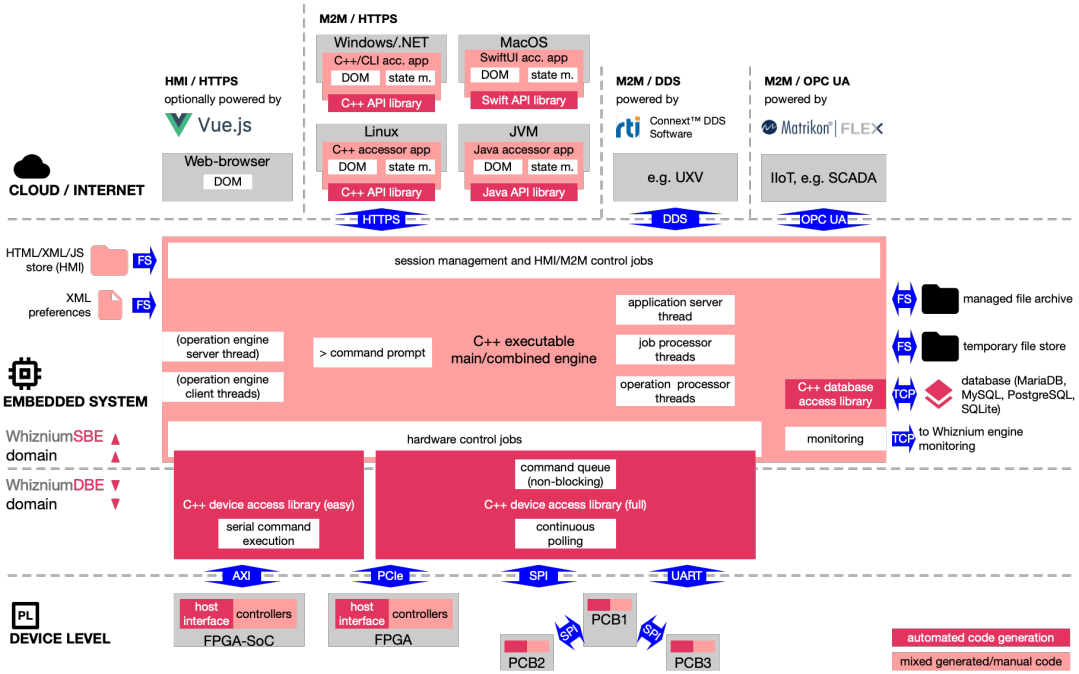
- “Database structure”: tables “Object group” (1:N) “Object” (1:N) “Snapshot” and corresponding ”Basic user interface”
- first “lowering” step: multi-locale UI elements, “queries”, “panels” and “controls”
- second “lowering” step: “blocks” and “dispatches” for engine <-> app communication
- code generation “database access library”
- code generation on engine side: classes for “cards”, ”panels” and ”queries” which at runtime dynamically generate objects responsible for web UI sessions and react to user input
- code generation app side: HTML and JavaScript

Conclusion demo project

The model-based approach pays off

- the maze of software technologies relevant for FPGA-SoC's is cleanly covered by a single, coherent method



Whiznium concepts

Modularity, transparency and re-usability

- Whiznium is Open Source; the generated code is subject to no license restrictions
- Whiznium generates well-organized, human-readable source code trees which can be synthesized / compiled “out-of-the-box”
- manual modifications are enabled through the concept of “insertion points”
- upon source code iteration (e.g. following model extension) manual modifications are carried over to the next version
- generated code relies on few, well-proven external libraries, all of which are Open Source. Standards are strictly followed
- WhizniumDBE features parametrized “module templates”. Besides corresponding VHDL files, template-specific intervention in the WhizniumDBE master database through C++ code is possible
- WhizniumSBE features parametrized “capability templates”. Also here, template-specific intervention in the WhizniumSBE master database through C++ code is possible

Whiznium tools

Incorporation into existing developer workflows

- WhizniumSBE and WhizniumDBE are Linux-based ”daemons” (and [fun fact] WhizniumSBE projects), which receive model information and send source code trees via HTTPS
- Java tools WhizniumDBE/SBE Bootstrap offer initialization of WhizniumDBE/SBE with project information stored in a local folder structure

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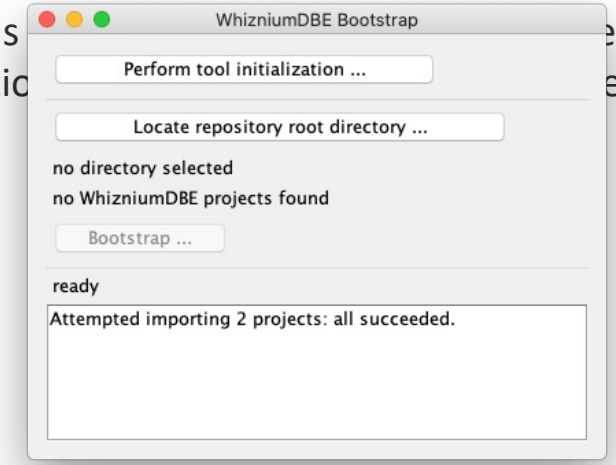

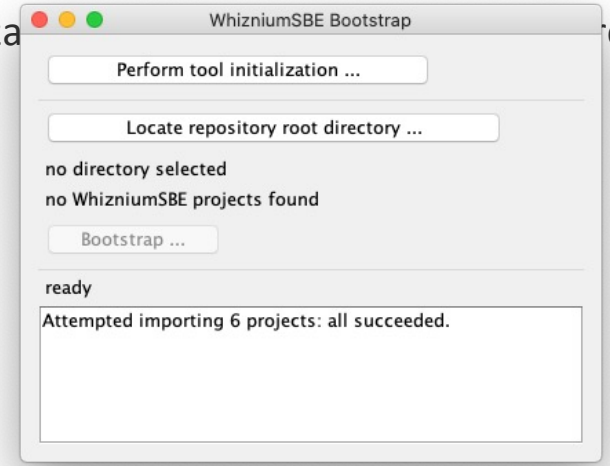

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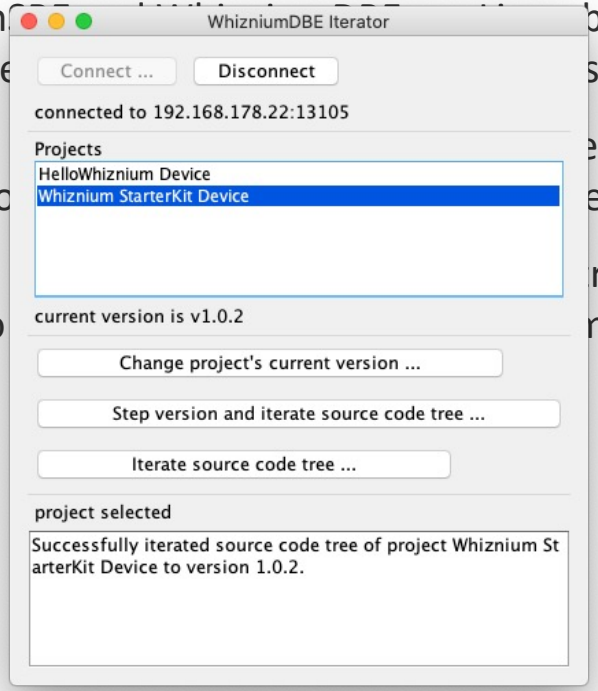

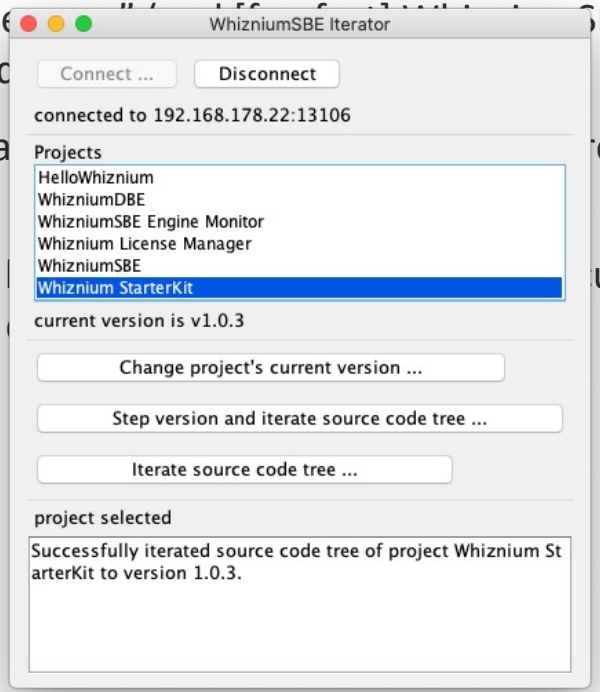

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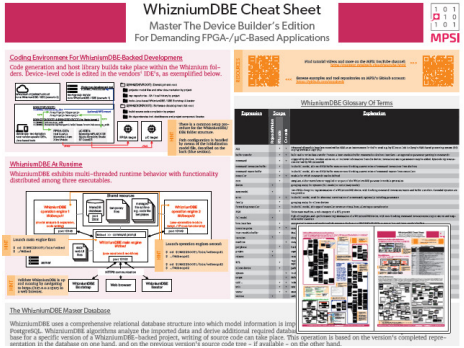
- WhizniumDBE code can be developed using the vendor-provided tools, e.g. Vivado, Quartus, Libero SoC or Simplicity Studio
- WhizniumSBE code can be (cross-)compiled using the industry-standard tool chains gcc/Clang. (Remote-)Debugging can be done using e.g. VS Code
- the Yocto project helps building custom Embedded Linux distributions for each FPGA-SoC platform. WhizniumSBE projects run on those distributions

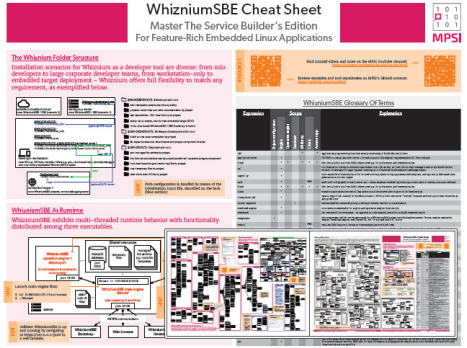
Resources

- both Whiznium tools are available free of charge on GitHub, including installation instructions

  https://github.com/mpsitech/The-Whiznium-Documentation

- the Open Source StarterKit ist available for various hardware platforms, with vendor-specific instructions also available on GitHub
- “The Whiznium Developer Experience” on YouTube is an ongoing Webinar series on Whiznium
- for advanced users WhizniumSBE/DBE cheat sheets are available which serve as reference for writing model files





Thank You!

Don’t hesitate to reach out

aw@mpsitechnologies.com